IN THE CLAIMS

Please amend the claims as indicated below.

1. (currently amended) An interlayer interconnection unit for a printed circuit board (PCB), comprising:

an interstitial bridge pad having a first side and a second side, wherein said first side of said interstitial bridge pad physically contacts a first dielectric layer and said second side of said interstitial bridge pad physically contacts a second dielectric layer;

a first blind via disposed on said first side of said interstitial bridge pad, wherein said first blind via extends through said first dielectric layer; and

a second blind via disposed on said second side of said interstitial bridge pad, wherein said second blind via extends through said second dielectric layer, wherein said interstitial bridge pad is adapted to electrically connect said first blind via to said second blind via,

wherein said interstitial bridge pad is coaxial in a z direction with said first blind via and with said second blind via, and

wherein, in the absence of an interstitial bridge pad therebetween, at least a portion of said first dielectric layer is fused to at least a portion of said second dielectric layer.

2. (original) The interlayer interconnection unit of claim 1, wherein said interstitial bridge pad comprises a disc-shaped conductive element.

3. (original) The interlayer interconnection unit of claim 1, wherein:

said first blind via extends from a first conductive layer, through said first dielectric layer, and to said first side of said interstitial bridge pad, and

said second blind via extends from a second conductive layer, through said second dielectric layer, and to said second side of said interstitial bridge pad.

4. (original) The interlayer interconnection unit of claim 1, wherein said first conductive layer and said second conductive layer each comprise copper foil.

5. (original) The interlayer interconnection unit of claim 1, wherein:

said first blind via extends from a first capture pad to said first side of said interstitial bridge pad, and

said second blind via extends from a second capture pad to said second side of said interstitial bridge pad.

6. (original) The interlayer interconnection unit of claim 5, wherein said first capture pad and said second capture pad each have a diameter less than a diameter of said interstitial bridge pad.

7. (original) The interlayer interconnection unit of claim 1, wherein said interstitial bridge pad has a diameter in the range of from about 12 to 20 mils.

8. (original) The interlayer interconnection unit of claim 1, wherein:

said PCB comprises a bridge layer disposed between said first dielectric layer and said second dielectric layer, and

said interstitial bridge pad is located within said bridge layer, and wherein said interstitial bridge pad lacks electrical connection, within said bridge layer, to a conductive element of said bridge layer.

9. (canceled)

10. (currently amended) An interlayer interconnection unit for a multi-layer PCB, comprising:

a first capture pad having a first annular ring;

a first via having a first via inner end and a first via outer end, said first via outer end in contact with said first capture pad and encircled by said first annular ring;

at least one interstitial bridge pad having a first side and a second side, said first via inner end in contact with said first side of said interstitial bridge pad;

a second via having a second via inner end and a second via outer end, said second via inner end in contact with said second side of said interstitial bridge pad; and

a second capture pad having a second annular ring, said second via outer end in contact with said second capture pad and encircled by said second annular ring,

wherein a first interstitial bridge pad of said at least one interstitial bridge pad lacks electrical connectivity to others of said at least one interstitial bridge pads, and.

wherein said first annular ring, said first via, said interstitial bridge pad, said second via, and said second annular ring are coaxial with each other.

11. (canceled)

12. (original) The interconnection unit of claim 10, wherein:
said first via extends through a first dielectric layer, and
said second via extends through a second dielectric layer.

13. (original) The interconnection unit of claim 10, wherein said interstitial bridge pad has a diameter in the range of from about 14 to 17 mils.

14. (original) The interconnection unit of claim 10, wherein:
said multilayer PCB comprises an internal bridge layer, and
said interstitial bridge pad is a component of said bridge layer.

15. (original) The interconnection unit of claim 10, wherein each of said first via and said second via has an aspect ratio of at least about 1:1.

16. (original) The interconnection unit of claim 10, wherein said interconnection unit has an effective aspect ratio greater than about 2:1.

17. (original) The interconnection unit of claim 10, wherein:

said first capture pad is located within a first conductive layer,

said second capture pad is located within a second conductive layer, and

said interconnection unit further comprises a third via extending from said first capture pad or said second capture pad to a third conductive layer.

18. (currently amended) A dual blind via interconnection unit for a multilayer PCB, comprising:

a pair of opposed coaxial blind vias transversing a pair of dielectric layers; and

at least one bridge pad disposed between said pair of blind vias, wherein each of said pair of dielectric layers is in physical contact with said bridge pad, and wherein said bridge pad is adapted to electrically interconnect said pair of opposed coaxial blind vias without electrically interconnecting any other blind vias,

wherein a first bridge pad of said at least one bridge pad lacks electrical connectivity to others of said at least one bridge pads.

19. (original) The interconnection unit of claim 18, wherein said bridge pad has a diameter in the range of from about 12 to 20 mils.

20. (original) The interconnection unit of claim 19, wherein each of said pair of blind vias has a diameter in the range of from about 4 to 6 mils.

21. (currently amended) A carrier for a multi-layer printed circuit board (PCB), said carrier comprising a pseudo three-layer core, said pseudo three-layer core including:

a first metal layer;

a first dielectric layer disposed on said first metal layer;

a bridge layer disposed on said first dielectric layer;

a second dielectric layer disposed on said bridge layer; and

a second metal layer disposed on said second dielectric layer,

wherein said bridge layer comprises a plurality of spaced apart interstitial bridge pads, and

wherein at least one of said plurality of interstitial bridge pads is adapted for providing an interlayer interconnection between said first metal layer and said second metal layer, and

wherein each of said plurality of interstitial bridge pads is physically connected to said first metal layer by a first blind via transversing said first dielectric layer, and

wherein each of said plurality of interstitial bridge pads is physically connected to said second metal layer by a second blind via transversing said second dielectric layer, and

wherein said interstitial bridge pad is coaxial in a z direction with said first blind via and with said second blind via, and

wherein, in the absence of an interstitial bridge pad therebetween, at least a portion of said first dielectric layer is fused to at least a portion of said second dielectric layer.

22. (canceled)

23. (original) The carrier of claim 21, wherein said bridge layer lacks an electrical connection between said plurality of interstitial bridge pads.

24. (original) The carrier of claim 21, wherein said plurality of interstitial bridge pads are spaced apart from each other by a distance in the range of from about 0.7 to 4 mils.

25. (original) The carrier of claim 24, wherein said plurality of interstitial bridge pads are arranged within said bridge layer at a center-to-center pitch in the range of from about 15 to 25 mils.

26. (original) The carrier of claim 21, wherein:

said first metal layer comprises a first signal layer of said PCB, and

said second metal layer comprises a second signal layer of said PCB.

27. (original) The carrier of claim 26, further comprising at least a third signal layer laminated to said pseudo three-layer core.

28. (original) The carrier of claim 26, wherein said carrier comprises from 2 to 4 additional signal layers laminated to said pseudo three-layer core.

29. (currently amended) A pseudo three-layer core for a printed circuit board (PCB), comprising:

a plurality of interlayer interconnection units, wherein each of said plurality of interlayer interconnection units extends from a first metal layer to a second metal layer;

a first dielectric layer disposed on said first metal layer;

a bridge layer disposed on said first dielectric layer; and

a second dielectric layer disposed on said bridge layer,

wherein said second metal layer is disposed on said second dielectric layer, and

wherein at least one of said plurality of interlayer interconnection units comprises:

an interstitial bridge pad located within said bridge layer;

a first blind via extending from said first metal layer to a first side of said interstitial bridge pad; and

a second blind via extending from said second metal layer to a second side of said interstitial bridge pad,

wherein said interstitial bridge pad is coaxial in a z direction with said first blind via and with said second blind via, and

wherein, in the absence of an interstitial bridge pad therebetween, at least a portion of said first dielectric layer is fused to at least a portion of said second dielectric layer.

30. (currently amended) A multi-layer printed circuit board (PCB), comprising:

a first signal layer;

a second signal layer;

a bridge layer disposed between said first signal layer and said second signal layer; and

a plurality of interlayer interconnection units, each of said plurality of interlayer interconnection units adapted for connecting said first signal layer with said second signal layer through said bridge layer, wherein at least one said plurality of interlayer interconnection units comprises:

a pair of opposed coaxial blind vias transversing a first dielectric layer and a second dielectric layer; and

a bridge pad physically contacting said first and second dielectric layers, said bridge pad in electrical contact with said pair of blind vias, and

wherein, in the absence of an interstitial bridge pad therebetween, at least a portion of said first dielectric layer is fused to at least a portion of said second dielectric layer.

31. (original) The multi-layer PCB of claim 30, wherein:

said bridge pad includes a first side and a second side; and wherein

said pair of opposed coaxial blind vias comprise a first blind via disposed on said first side of said bridge pad, and a second blind via disposed on said second side of said bridge pad.

32. (original) The multi-layer PCB of claim 30, further comprising at least one additional dielectric layer laminated to said first signal layer, and at least one additional signal layer laminated to said at least one additional dielectric layer.

33. (currently amended) A multi-layer PCB, comprising:

at least one pseudo three-layer core including:

a first metal layer;

a first dielectric layer disposed on said first metal layer;

a bridge layer disposed on said first dielectric layer;

a second dielectric layer disposed on said bridge layer;

a second metal layer disposed on said second dielectric layer; and

a plurality of interlayer interconnection units for electrically interconnecting said first metal layer with said second metal layer, wherein at least one of said plurality of interlayer interconnection units comprises:

an interstitial bridge pad having a first side and a second side;

a first blind via disposed on said first side of said interstitial bridge pad extending through said first dielectric layer; and

a second blind via disposed on said second side of said interstitial bridge pad extending through said second dielectric layer,

wherein said interstitial bridge pad is coaxial in a z direction with said first blind via and with said second blind via, and

wherein, in the absence of an interstitial bridge pad therebetween, at least a portion of said first dielectric layer is fused to at least a portion of said second dielectric layer.

34. (original) The multilayer PCB of claim 33, wherein each of said plurality of interlayer interconnection units is adapted for electrically interconnecting said first metal layer with said second metal layer.

35. (original) The multilayer PCB of claim 33, wherein:

each of said first metal layer and said second metal layer comprises a signal layer, and

said multilayer PCB further comprises at least one additional signal layer laminated to said at least one pseudo three-layer core.

36. (original) The multilayer PCB of claim 33, wherein said at least one pseudo three-layer core comprises a first pseudo three-layer core and at least a second pseudo three-layer core laminated to said first pseudo three-layer core.

37. (original) The multilayer PCB of claim 33, wherein said multilayer PCB comprises from 1 to 4 pseudo three-layer cores and from 4 to 28 signal layers.

38. (currently amended) A multilayer PCB, comprising:

means for carrying a plurality of signal layers; and

means for interconnecting at least two of said plurality of signal layers,

wherein said carrying means comprises a pseudo three-layer core,

wherein said pseudo three-layer core includes an internal bridge layer that comprises a plurality of interstitial bridge pads, a first dielectric layer, and a second dielectric layer, and

wherein said interconnecting means comprises a pair of opposed blind vias disposed on either side of each of said plurality of interstitial bridge pads, said pair of opposed blind vias transversing said first and second dielectric layers, and

wherein said interstitial bridge pad is coaxial in a z direction with said first blind via and with said second blind via, and

wherein, in the absence of an interstitial bridge pad therebetween, at least a portion of said first dielectric layer is fused to at least a portion of said second dielectric layer.

39. (original) The multilayer PCB of claim 38, wherein:

said bridge layer comprises an internal pseudo metal layer disposed between a first dielectric layer and a second dielectric layer, and

wherein said interconnecting means is adapted for interconnecting said plurality of signal layers.

40. (currently amended) A method for forming a multilayer printed circuit board (PCB), comprising:

a) providing a metal clad first dielectric layer having a first metal clad side and a second metal clad side;

b) forming a bridge layer from said second metal clad side, wherein said bridge layer comprises a plurality of bridge pads disposed on said first dielectric layer, and wherein said first metal clad side comprises a first metal layer;

c) providing a second dielectric layer disposed on said bridge layer, wherein said second dielectric layer has a second metal layer disposed thereon;

d) forming a first blind via through said first dielectric layer, wherein said first blind via extends from said first metal layer to a first side of at least one of said plurality of bridge pads; and

e) forming a second blind via through said second dielectric layer, wherein said second blind via extends from said second metal layer to a second side of said at least one of said plurality of bridge pads,

wherein said bridge pad is coaxial in a z direction with said first blind via and with said second blind via, and

wherein, in the absence of an interstitial bridge pad therebetween, at least a portion of said first dielectric layer is fused to at least a portion of said second dielectric layer.

41. (original) The method of claim 40, wherein said step b) comprises etching said second metal clad side of said first dielectric layer to form said at least one of said plurality of bridge pads.

42. (original) The method of claim 40, wherein:

said second metal clad side comprises copper foil, and

wherein said at least one of said plurality of bridge pads comprises copper.

43. (original) The method of claim 40, wherein each of said plurality of bridge pads has a diameter in the range of from about 12 to 20 mils.

44. (original) The method of claim 40, wherein said bridge layer lacks electrical connectivity between said plurality of bridge pads.

45. (original) The method of claim 40, wherein said steps c) and d) respectively comprise forming said first blind via and said second blind via by a process selected from the group consisting of laser drilling, plasma drilling, and photo-defining.

46. (original) The method of claim 40, further comprising:

e) plating shut said first blind via and said second blind via.

47. (original) The method of claim 40, wherein said method involves only a single plating cycle.

48. (original) The method of claim 46, wherein after said step e), said first metal layer and said second metal layer each have a thickness in the range of from about 0.8 to 1.4 mils.

49. (original) The method of claim 46, wherein after said step e) said first metal layer and said second metal layer each have a thickness in the range of from about 0.9 to 1.1 mils.

50. (original) The method of claim 40, wherein said first blind via and said second blind via each comprise a μvia having a diameter in the range of from about 4 to 5 mils.

51. (currently amended) A method for forming a multilayer printed circuited board (PCB), comprising:

a) forming a pseudo three-layer core, said pseudo three-layer core including:

a first metal layer;

a first dielectric layer disposed on said first metal layer,

a plurality of spaced apart interstitial bridge pads ~~a bridge layer~~ disposed on said first dielectric layer;

a second dielectric layer disposed on said plurality of spaced apart interstitial bridge pads ~~bridge layer~~; and

a second metal layer disposed on said second dielectric layer~~, wherein said bridge layer comprises a plurality of spaced apart interstitial bridge pads~~; and

b) forming a plurality of interlayer interconnection units for interconnecting said first metal layer and said second metal layer, wherein each of said interlayer interconnection units includes:

a first blind via disposed on a first side of one of said plurality of interstitial bridge pads, wherein said first blind via extends from said first metal layer through said first dielectric layer; and

a second blind via disposed on a second side of one of said plurality of interstitial bridge pads, wherein said second blind via extends from said second metal layer through said second dielectric layer, wherein said interstitial bridge pad is coaxial in a z direction with said first blind via and with said second blind via.

52. (original) The method of claim 51, wherein:

said step b) comprises plating shut said first blind via and said second blind via, and

said method includes only a single plating cycle.

53. (original) The method of claim 51, wherein each of said first blind via and said second blind via has an aspect ratio of at least about 1:1.

54. (original) The method of claim 53, wherein each of said interlayer interconnection units has an effective aspect ratio of at least about 2:1.

55. (original) A method for forming a multilayer printed circuit board (PCB), comprising:

a) a step for forming a pseudo three-layer core, wherein said pseudo three-layer core includes:

a first metal layer;

a first dielectric layer disposed on said first metal layer;

a plurality of bridge pads ~~a bridge layer~~ disposed on said first dielectric layer;

a second dielectric layer disposed on said bridge pads ~~bridge layer~~; and

a second metal layer disposed on said second dielectric layer; and

b) a step for forming a plurality of interlayer interconnection units for electrically interconnecting said first metal layer and said second metal layer, wherein each of said interlayer interconnection units includes:

a pair of opposed coaxial blind vias, and

one of said plurality of bridge pads ~~a bridge pad~~ disposed between, and in electrical contact with, said pair of blind vias~~, wherein said bridge layer comprises a plurality of said bridge pads~~.

56. (currently amended) A method for forming a pseudo three-layer core for a PCB, comprising:

a) providing a first metal layer;

b) providing a first dielectric layer on said first metal layer;

c) forming a plurality of bridge pads ~~bridge layer~~ on said first dielectric layer~~, said bridge layer comprising a plurality of bridge pads~~;

d) providing a second dielectric layer on said plurality of bridge pads ~~bridge layer~~;

e) providing a second metal layer on said second dielectric layer;

f) forming a first blind via on a first side of each of said plurality of bridge pads, wherein said first blind via extends from said first metal layer through said first dielectric layer; and

g) forming a second blind via on a second side of each of said plurality of bridge pads, wherein said second blind via extends from said second metal layer through said second dielectric layer,

wherein each of said plurality of bridge pads is coaxial in a z direction with said first blind via and with said second blind via.

57. (original) The method of claim 56, wherein:

said first dielectric layer comprises a first side and a second side, said first side having said first metal layer disposed thereon, and said second side having a layer of copper foil disposed thereon, and

said step c) comprises etching said layer of copper foil.